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Proposal of an analog IC fault model and an analog IC board fault detection using supply current

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Abstract-By making a discrete circuit of a typical Op-amp internal circuit, the IC Op-amp's fault modes were investigated. The results of the experiment showed that the Op-amp's internal transistor fault was represented by the supply current's abnormal value. Next, the experiment was performed in six ways to simulate the fault that occurred in the actual IC Op-amp and simulation circuit. From the results of the experiment, this paper proposes the fault model of an Op-amp. After these results, this paper obtained a fault detection rate of approximately 86%. This paper then proposes a current sensor that has an LED to designate a fault, thus making this sensor effective in the fault detection of board level and the mixed signal LSI. Thus a maintenance engineer can easily and quickly diagnose the fault point, to enable the change in board or the LSI. The results of this paper verified the usefulness of the supply current test to detect faults in analog circuits.

Index terms-Analog IC, analog circuit, analog board, Op-amp, fault detection, mixed signal LSI

I. Introduction

Fault detection and diagnosis methods in digital circuits have long been established. These methods have been applied to many kinds of circuits. However, the same could not be said in the analog circuit case due to the variety of circuits available. Analog circuit fault detection and diagnosis methods have been discussed recently by [1], [2],[3] and [4]. In this paper, a standard IC used in analog circuits, the Op Amp in its fault mode will be discussed. Circuit simulation is usually used to analyze the circuit in the fault mode, however, in this paper, a discrete circuit will be partly used instead. Because a fault occurs accidentally, therefore, it cannot be realized favorably by simulation. For example, a transistor is destroyed, and an input terminal wiring pattern is dissolved by the accidental outside noise.

When a discrete Op Amp is implemented, the transistor size, the line width and length of the internal circuit connection, as well as the delay time would be different from the actual IC Op-amp. However, since this paper will only discuss surge fault detection, these differences would not matter. This paper assumes that defects such as internal circuit connection shorts or transistor faults do not occur in the manufacturing process. Moreover surge faults only occur in the user's side. In the surge fault mode, damage is done to the oxide film insulation and to the p-n junction. Moreover, there is melting in the internal aluminum circuit. On the user's side, the following could be considered the causes that results to defective ICs: intrusion of static electricity, a miss operation resulting in high voltage supplied to the chip, surge voltage generated by the on and off switching of other equipment. Most recently, almost all analog circuits have been implemented using IC-Op-amp. Thus, in this paper, three analog circuits were constructed on the PCB.In the above surge experiment, a defective IC Op-amp was used and the supply current experiment was performed at the board level. Six analog circuits were simulated by P-spice for the fault detection experiment using the supply current. Moreover, this paper performed the actual experiment using the actual fault IC Op-amp to the two kinds circuits.

Collecting this paper performed the following experiments.

1.IC Op-amp fault :3.1,3.2
→fault detection rate of actual IC board :7
→fault trend→fault model (open/short/transistor fault) :4,5
2.IC Op-amp input open:3.2
3.The fault detection rate of the discrete and simulation :7

From the experiment results, this paper proposed the fault model of an Op-amp. After these results, this paper obtained the fault detection rate to the analog board. This paper then proposed a current sensor for the fault detection. This sensor is effective in fault detection at the board level and the mixed signal LSI, because the maintenance engineer can easily and quickly diagnose the fault point, thus anyone can change the board or the LSI.

2. Fundamental principle

The transistors are added a bias to the active region in an analog circuit. Therefore there is no input, a collector current and a base current always flow through the circuits. In other words a supply current in an analog IC always flows through the whole circuit without an input. The IC Op-amp 741 is composed by 20 transistors, hence these supply currents are flowing through the circuits. Therefore, if this supply current change exceeds the normal range, fault detection becomes possible. Similarly, for this result, the fault detection of an analog board can be performed using the total supply current.

As previously mentioned, when supply current appears to change, this phenomenon could be used shows a fault in a circuit without input.

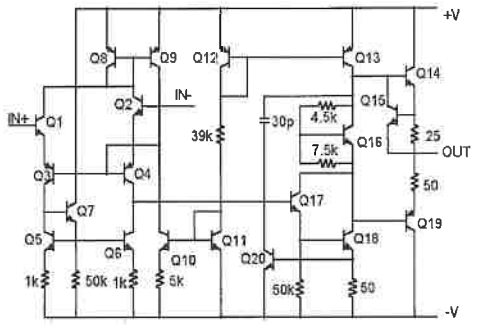
3. IC Op-amp

3.1 Fault discussion of IC Op-amp

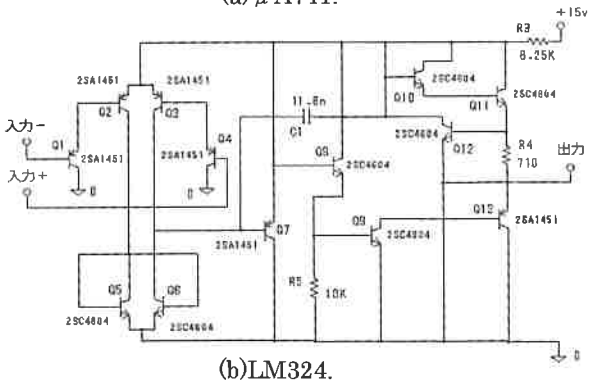
The μA741 is reliable and generally used and the LM324 is single power supply an Op-amp. Those internal circuits are shown in **Fig.1**. In order to discuss these IC Op-amp fault conditions, the μA741 Op Amp and its discrete equivalent is both configured as a 0dB invert circuit of **Fig. 2.** Steps 1) and 2) is first applied to the μA741 Op-amp as mentioned in the procedure below, as follows:

Experimental procedure:

1) Supply a high voltage to each IC Op-amp terminal to destroy the IC.
2) On another IC, leave each IC pin unconnected one at a time to simulate an open condition.



(a) μA741.



(b)LM324.

Fig.1 IC Op-Amp.

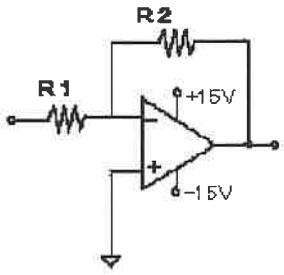


Fig.2 Invert amplifier.

3.2 Actual IC Op-amp fault experiment

The following nine fault experiments were performed to simulate an IC Op-amp that is destroyed, in many cases, by a surge current at the user's side.

A: Apply a ±35V at the power supply terminal
B: Apply a ±45V at the power supply terminal
C: Apply a ±55 at the power supply terminal
D: Apply an inverse ±15V at the power supply terminal
E: Apply ±50 V between pins 2 and 5
F: Apply ±50 V between pins 7 and 6
G: Apply ±50 V between pins 3 and 6
H: Apply ±50 V between pins 6 and 4
I: Apply ±50 V between pins 3 and 1

Table 1 shows the supply current and output voltage of the nine ICs above in an inverting circuit of Fig.2. In this table, when pin 7 (+ voltage terminal) and pin 4 (− voltage terminal) was supplied an over voltage, the positive (+) and the negative (-) supply current for chips A, B, C, D,F and H resulted in a zero current in either or both cases.

Table 1 Supply current using defective IC Op-Amp.

Actual circuit.
Non-fault: +2.10[mA],-2.10[mA]

No,	Supply Current	
	I+[mA]	I−[mA]
A	0.00	−3.19
B	0.00	−5.12
C	0.00	−3.96
D	0.00	−3.22
E	1.20	−9.87
F	0.00	0.00
G	6.66	−1.12
H	0.00	0.00
I	0.27	−4.89

3.3 IC Op-amp's terminal open

Table 2 mentioned below, shows the case in which each terminal of the IC Op-amp is open. A ↓ shows that the supply current decreased and a ↑ shows that supply current increased in Table 1 (b). And, a (-) shows that the supply current did not change. From **Table 2 (b)**, if the even one tendency ↑ ↓ − (this case will be shown in table 4) of a result of the simulation agrees with the result of the actual circuit,

the fault tendency of the actual circuit corresponds to the simulation in the supply current of the fault situation. These parts are shown in **Table 2 (b)** by the no white cutout part. While the white cutout part in the table is when the result is not in the inclusion relations.

Table 2 Case of each terminal open.

(a)Experiment result.

	Simulation		Actual circuit	
pinNo	I+[mA]	I−[mA]	I+[mA]	I−[mA]
2	21.41	−0.79	6.70	−1.19
3	1.68	−20.66	1.45	−6.30
4	14.47	0.00	4.05	0.00
6	0.80	−0.80	1.71	−1.71
7	0.00	−3.17	0.00	−6.25
2 3	21.37	−0.74	6.60	−1.09
2 4	14.47	0.00	4.06	0.00
2 6	0.79	−0.79	1.24	−1.24
2 7	0.00	−3.17	0.00	6.57
3 4	14.47	0.00	4.06	0.00
3 6	1.71	−1.70	2.04	−2.04
3 7	0.00	−19.20	0.00	−5.29
4 6	0.00	0.00	0.00	0.00
4 7	0.00	0.00	0.00	0.00
6 7	0.00	0.00	0.00	0.00

(b) Comparison of trend.

PinNo.	Simulation		Actual circuit	
	I+[mA]	I−[mA]	I+[mA]	I−[mA]
2	↑	↑	↑	↑
3	↑	↓	↓	↓
4	↑	↑	↑	↑
6	↓	↑	↓	↑
7	↓	↓	↓	↓
2 3	↑	↑	↑	↑
2 4	↑	↑	↑	↑
2 6	↓	↑	↓	↑
2 7	↓	↓	↓	↓
3 4	↑	↑	↑	↑
3 6	↑	↓	↓	↑
3 7	↓	↓	↓	↓
4 6	↓	↑	↓	↑
4 7	↓	↑	↓	↑
6 7	↓	↑	↓	↑

When pin 7 (+ voltage terminal) is made open, the Op Amp will have the same condition (+ supply current is zero) as Op-amp A, B, C and D which was applied an over voltage in the power supply terminal.

When pin 6 (output) and pin 7 (+ voltage terminal) is made open, the IC Op-amp will have the same condition (± supply current is zero) as IC Op-amp F. The above mentioned case results when the supply terminal is applied an over voltage, melting the internal aluminum connection to the power supply terminal, resulting to a disconnection of the supply voltage and ／ or also causing damage to the surrounding transistors.After applying an over voltage to the input/output terminal (pin 2,3), and the offset adjust terminal (pin 1, 5), the Op Amp will have the same fault condition as above. In the IC Op-amp E, G and I, after an over voltage was applied to the input-output (pin 2, 3) and offset adjust terminals (pin 1, 5), an abnormal amount of current flowed that damaged the IC Op-amps internal transistor. **Fig. 3** shows the internal pattern condition of a defective IC Op-amp C.

In the above mentioned IC Op-amp's fault detection experiment, melting of the supply voltage terminal occurs when the supply voltage terminal was applied an over voltage.To simulate this condition using the actual IC Op-amp and P-spice simulation, the individual terminals in Table 2 were opened. Table 2 (b) shows the trend of the supply current (increase/decrease).Then the supply current and the output were measured. When pin 4 and 7 of the IC Op-amps in Table 2 were opened, with the supply current becoming almost zero (0.00), it can be concluded that melting occurred in the internal aluminum connection to the supply voltage terminal.

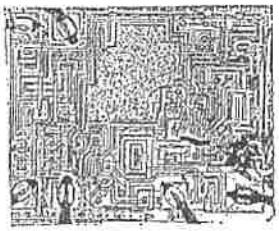


Fig.3 Defective IC's internal print pattern.

4. Transistor fault in an actual circuit

When a suitable bias between the base-emitters of the transistor (NPN: 2SC380, PNP: 2SA561) is applied to put the transistor into the on state, an over current added by the over collector voltage puts the collector-emitter. The fault condition of the transistor is shown as follows:

- 2SC380 collector-emitter :Open
  base-emitter :Open
  base-collector : 2～4kΩ
- 2SA561 collector-emitter :Open
  base-emitter :Open
  base-collector :0.7～0.9kΩ

The input resistance of a transistor is low and the output resistance is high. When a transistor is destroyed by the over current, the base-emitter-side becomes open and the output side becomes several k ohm about the actual transistor fault. Because transistor input resistance is low and output resistance is high.

Table 3 Result of simulation and experiment.

(a) μA741.

Simulation Non-fault: +1.6[mA],-1.6[mA]

Actual circuit +2.10[mA],-2.10[mA]

Tr	Simulation						Actual circuit					
	OPEN		SHORT		Tr fault		OPEN		SHORT		Tr fault	
	I+[mA]	I−[mA]	I+[mA]	I−[mA]	I+[mA]	I−[mA]	I+[mA]	I−[mA]	I+[mA]	I−[mA]	I+[mA]	I−[mA]
Q1-NPN	166	−19.56	322[A]	−19.40	28.55	−0.76	large	large	2.87	−8.02	6.99	−0.76
Q2-NPN	21.76	−1.34	38.59	−32.67	22.94	−0.76	9.96	−0.76	6.24	−0.74	9.46	−0.76
Q3-PNP	1.66	−19.56	27.55	−45.50	1.83[A]	1.84[A]	large	large	2.77	−7.92	large	large
Q4-PNP	21.76	−1.38	21.76	−1.33	8.27[A]	8.31[A]	large	large	6.30	−0.80	large	large
Q5-NPN	5.42	−19.56	21.76	−1.33	1.59	−1.67	2.09	−2.22	4.76	−1.60	2.10	−2.03
Q6-NPN	21.76	−1.33	1.68	−19.40	21.41	−0.78	6.34	−0.78	2.09	−2.22	6.29	−0.78
Q7-NPN	21.76	−1.33	60.65	−78.55	21.41	−0.76	large	large	2.04	−2.18	6.45	−0.85
Q8-PNP	21.76	−1.33	21.76	−1.33	1.64	−1.58	large	large	3.03	−8.16	6.27	−0.76
Q9-PNP	4.33	−22.24	1.66	−19.56	21.41	−0.76	large	large	84.50	−89.60	6.27	−0.76
Q10-NPN	1.64	−19.50	13.7[A]	13.9[A]	525.00	−543.00	large	large	6.24	−0.74	3.21	−3.24
Q11-NPN	6.00	−22.96	1.68	−19.56	14.31	−32.77	6.30	−0.76	6.10	−11.30	5.92	−11.20
Q12-PNP	22.00	−1.33	0.80	−10.85	32.29	−11.68	0.80	−0.83	20.50	−15.20	20.30	−15.10
Q13-PNP	0.78	−10.85	21.99	−1.35	31.30	−11.68	20.50	−15.10	0.79	−0.82	20.50	−15.40
Q14-NPN	1.33	−1.34	22.96	−1.34	0.80	−0.80	30.60	−25.00	2.05	−2.10	2.29	−2.32
Q15-NPN	1.60	−1.67	1.62	−6.65	1.60	−1.60	2.00	−2.05	2.17	−2.17	2.05	−2.69
Q16-NPN	26.39	−17.96	21.15	−1.34	26.24	−26.24	2.05	−2.08	29.20	−29.20	29.20	−29.30
Q17-NPN	1.69	−19.56	21.76	−1.33	21.41	−0.76	2.57	−8.09	6.72	−1.21	6.74	−1.23
Q18-NPN	21.76	−1.33	1.70	−21.59	21.84	−1.31	2.68	−7.94	6.29	−0.76	4.81	−1.69
Q19-PNP	1.60	−1.67	1.70	−22.63	1.70	−20.63	6.90	−12.70	2.01	−2.03	20.50	−7.55
Q20-NPN	1.60	−1.67	1.70	−20.69	21.41	−0.78	6.33	−0.78	2.13	−2.15	6.28	−0.77

(b) LM324.

Non-fault: +1.6[mA]

Tr	OPEN	SHORT
	V+(mA)	V+(mA)
Q1	2.28	0.94
Q2	2.28	0.84
Q3	0.90	2.01
Q4	0.90	2.01
Q5	1.55	2.28
Q6	2.28	0.84
Q7	2.28	0.84
Q8	0.84	2.29
Q9	0.89	2.04
Q10	0.95	1.63
Q11	0.95	1.83
Q12	1.66	1.92
Q13	2.04	2.12

Table 4 Trend of result.

Tr	Simulation						Actual circuit					
	OPEN		SHORT		Tr故障		OPEN		SHORT		Tr故障	
	V+	V−	V+	V−	V+	V−	V+	V−	V+	V−	V+	V−
1	↑	↓	↑	↓	↑	↑	↑	↓	↑	↓	↑	↑
2	↑	↑	↑	↓	↑	↑	↑	↑	↑	↑	↑	↑
3	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓
4	↑	↑	↑	↑	↑	↓	↑	↓	↑	↑	↑	↓
5	↑	↑	↑	↓	—	—	—	↓	↑	↑	—	↑
6	↑	↓	↑	↓	↑	↑	↑	↓	—	↑	↑	↓
7	↑	↑	↑	↓	↑	↑	↑	↓	↑	↓	↑	↑
8	↑	↑	↑	↓	—	—	↑	↓	↑	↓	↑	↑
9	↑	↑	↑	↓	↑	↑	↑	↓	↑	↓	↑	↑
10	—	↓	↑	↓	↑	↓	↑	↓	↑	↑	↑	↓
11	↑	↓	↑	↓	↑	↓	↑	↑	↑	↓	↑	↓
12	↑	↑	↓	↓	↑	↓	↓	↑	↑	↓	↑	↓
13	↓	↓	↑	↑	↑	↓	↑	↓	↓	↑	↑	↓
14	—	—	↑	↓	↓	↑	↑	↓	—	—	↑	↓
15	—	—	—	↓	—	—	↓	—	↑	↓	—	↓
16	↑	↓	↑	↑	↑	↓	—	—	↑	↓	↑	↓
17	↑	↓	↑	↑	↑	↑	↑	↓	↑	↑	↑	↑
18	↑	↑	↑	↓	↑	↑	↑	↓	↑	↑	↑	↑
19	—	—	↑	↓	↑	↓	↑	↓	↓	↑	↑	↓
20	—	—	↑	↓	↑	↑	↑	↑	—	—	↑	↑

It is mounted on the transistor Q1～Q20 of the discrete 741 Op-amp which assembled this fault transistor the one after another. When a 0dB invert circuit was assembled, the supply current is shown in **Table 3 and 4**. At once, Pspice simulation results were shown in that table. These experiments were performed by an open,short and transistor fault (Tr fault) in Fig4. When an inside transistor breaks down, it is understood that increase (or, decrease) in current shows a tendency to have either supply current both from (+ or -) Table 4.

5 The proposal of fault model of the Op-amp

Table 5 shows that the relationship between the open fault, short fault and transistor fault in the condition of the supply current in the fault experiment of six circuits using the fault model of **Fig.4**. This table shows that the 91.5% of the transistor fault is contained in the open and short fault of the transistor. At this point, it was shown that the propriety of the actual fault detection could be determined by doing only an open and short fault experiment or simulation..It confirmed with the actual circuit and with the simulation.

Table 5 Containment rate.

No.	Circuit	Containment rate [%]
1	Voltage follower	95.0
2	Invert circuit	85.0
3	Audio oscillator	95.0
4	Sine oscillator	97.5
5	Peak detector	85.0
6	Active filter	91.3
Total		91.5

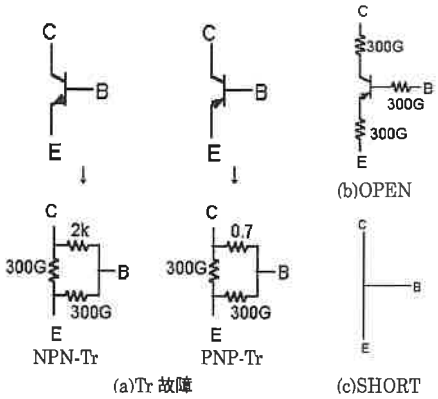


Fig.4 Fault model for transistor.

This paper performed the fault detection experiment using those fault transistor model (Fig.4) of the actual IC Op-amp and the P-spice simulation in Table 5. Consequently, this resulted into **Fig.5**, this fact shows that an open fault and short fault includes about 91%of transistor faults.From the fault experiment of 3.12 and 3.13, 4.1the fault occurring in the IC Op-amp at the user's side can be considered to have the following conditions:

(l) The internal aluminum connection to the power supply terminal melts when the supply voltage terminal is applied an over voltage, disconnecting the voltage supply to the internal circuit.
(2) When the input／output terminal is applied an over voltage, the internal transistors are destroyed, resulting to the decrease and increase of the positive or supply current below or beyond its normal value.

These discussions prove that the open and short transistor fault model is enough in a fault detection simulation.

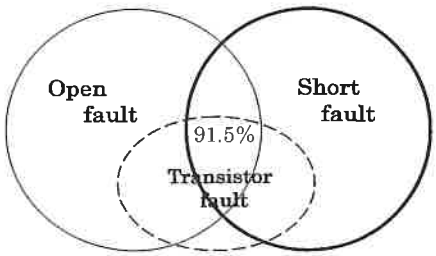


Fig.5 Open and short relationship with transistor fault.

6. Threshold Level

The IC Op-amp supply current varies according to the ambient temperature and the IC characteristics. Thus, by constructing an inverted IC Op-amp using Fig 2, measuring the supply current and varying the temperature range from 10 ℃ to 40 ℃, the supply current, as shown in (1) is a random variable x having a normal distribution with a mean μ and a standard deviation σ,

$$y(x)=\frac{1}{\sqrt{2\pi}\sigma}\exp(-\frac{(x-\mu)^2}{2\sigma^2}) \qquad (1)$$

letting x = I, the threshold range is determined to be,

$$\mu-3\sigma<I<\mu+3\sigma \qquad (2)$$

The following are the results for μ and σ,

[Positive supply current]: $\mu+=2.07$ [mA]
$\sigma+=0.20$ [mA]

[Negative supply current]: $\mu - = -2.07$[mA]
$\sigma - = 0.20$[mA]

Thus, in the normal operation, the supply current range is,

$$1.47 < I < 2.67 \quad [mA] \quad (3)$$

Using the threshold range in equation (3) on the results of the previous open or shorted transistor fault experiment, the single defective transistor fault experiment which had 60 combinations, resulted in a fault detection rate of about 85%.

7. Fault detection experiment of analog boards

When a fault in the user's side occurs, this can be due to one or more causes. The application of an over voltage, the change in the ambient temperature, moisture, or surge voltages generated by the surrounding equipment, influences the IC Op-amp to be at the fault condition. Since a computer simulation to duplicate the environment that caused the fault condition at the user's side is not possible, it is necessary to simulate the fault condition by actually constructing the circuit and insert defective IC Op-amps.

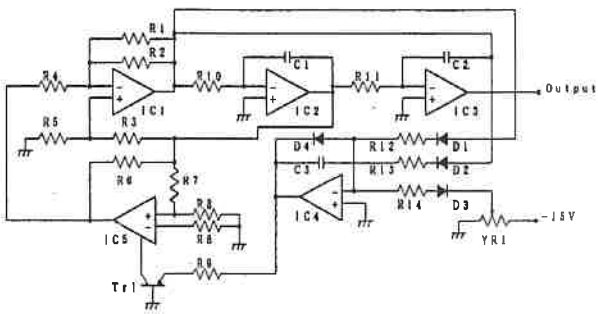


Fig.6 Sine wave oscillator.

The experiment was performed by constructing three analog boards using μ A741 and applying fault conditions A to I as shown previously in Table I. Shown in **Fig.6** is the sine wave oscillation circuit. In Fig 6, if the 4 IC Op-amps IC1 to IC4 (except IC5) are replaced one at a time with a defective IC (case A to I in Table 1), a circuit with 36 different fault combinations can be obtained. The supply current result in this experiment can be graphically depicted as shown in **Fig.7**.

The threshold range in this case was determined to be,

[Positive supply current]: $8.26 < I < 10.3$ [mA]
[Negative supply current]: $9.68 < I < 11.7$ [mA]

In Fig.7, it can be seen that of the 36 different fault combinations, 2 cases (black bars) occur wherein both the positive and negative supply currents fell with in the threshold range. The resulting fault detection rate was computed to be 94.4% (34/36). However, the result of this circuit in the simulation of the transistor fault was 85.5%.

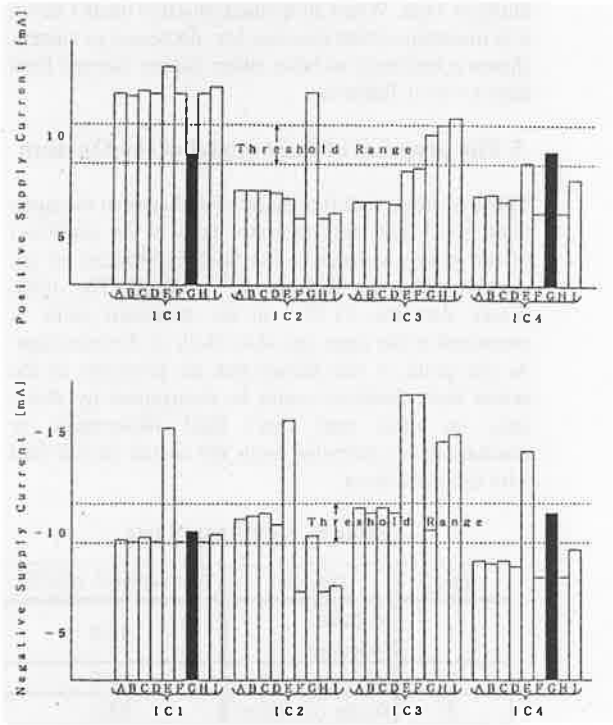


Fig.7 Graphical representation of the supply current result.

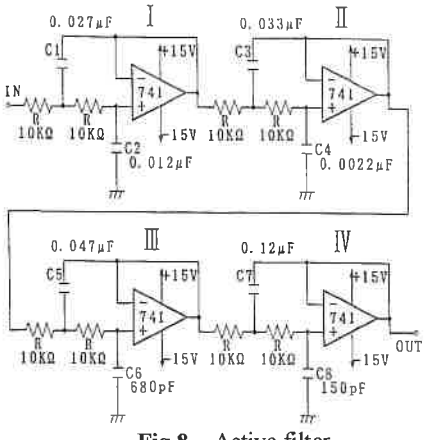


Fig.8 Active filter.

Using 4 faults Op-amps in a filter circuit as shown in Fig.8, the same experiment as in the previous circuit was performed.

Table 6 shows that the results of a fault detection experiment of six kinds of analog IC boards by the open, short and transistor fault inserting. Four of the four boards (1,2,4,6) in table 6 had the experiment done by both the actual circuit and the simulation. The result of the fault detection rate in that case almost had the same results in both experiment. The other two remaining boards were only simulated, and a fault detection experiment was done. As for the fault of the transistor, it was found that about 86% could be detected by the supply current from the **Table 6**.

Table 6 Fault detection rate.

No.	Circuit	Tr fault [%]	OPEN [%]	SHORT [%]	Op Amp
1	Voltage follower	85.0	75.0	85.0	1
2	Invert circuit	85.0	80.5	100.0	1
3	Audio oscillator	87.5	75.0	90.0	4
4	Sine oscillator	85.0	67.5	85.0	5
5	Peak detector	85.0	100.0	100.0	6
6	Active filter	91.3	91.3	90.0	4
Total		86.4	81.6	91.7	
			86.7		

8. Supply current test limit of board or mixed signal LSI

Increasing the number of ICs on the board inevitably increases the supply current thus, widening the threshold level. Consequently, even if the IC is defective, and the variation in the supply current falls within the threshold range, it is not possible to detect the fault. Hence, this paper theoretically discusses the limits in the supply current fault detection method. Assume that the IC Op-amp's supply current is a normal distribution. When n is the number of IC Op-amps on the PCB, M is the mean of the total board supply current and s the standard deviation. When each IC Op-amp's mean is μ_i and standard deviation σ_i, (i = 1 , 2 , ・・・n), by statistical theory:

$$M = \sum_{i=1}^{n} \mu_i \tag{9}$$

$$\sigma = \sqrt{\sum_{i=1}^{n} \sigma_i^2} \tag{10}$$

Assuming that the IC Op-amps are all of the same type, equation (9) and (10) becomes

$$M = n\mu \tag{11}$$

$$s = \sqrt{n}\sigma \tag{12}$$

For the non fault ICs, the supply current threshold range is:

$$M = \pm 3s \tag{13}$$

Using equation (12) and (13),

$$3s = 3\sqrt{n}\sigma \tag{14}$$

When the supply current is larger than 3s of equation (14), it is possible to detect faults. Assume I_F to be the total supply current. When one of the n Op Amps is at the fault condition, with I* increasing or decreasing in value, and falls within the 3s range, it is not possible to detect the fault. Thus, the limit of fault detection becomes

$$3\sqrt{n}\sigma = I_F \tag{15}$$

Using equation (12), with σ (=0 2) and μ ($=I_F$=2 07) of the piecewise linear circuit, n is calculated to be 11 ICs. This result means that if the number of ICs is more than 11, it is not possible to detect the fault.

As shown in chapter 3, the measured value of σ is smaller than the computed value by about 70%. Using this fact to calculate n, the value of n = 36 chips is obtained. If the number of ICs is more than 11, equation (15) becomes

$$3\sqrt{n}\sigma < I_F \tag{16}$$

The n and I_F relationship with varying values of the c parameter is shown in **Fig.9**. This figure shows that the threshold range increases as the number of ICs n increases, making it difficult to detect faults.

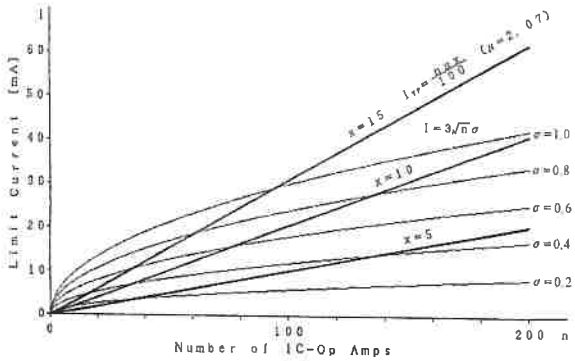


Fig.9 Threshold level comparison.

9. Comparison of threshold level

Setting the threshold level mean μ equal to I_{TP} (standard current value), assuming a threshold level of $\pm$x% about the mean μ, and n the number of IC Op-amps on the PCB, the absolute value of the threshold level μ x／100 becomes,

$$I_{TP} = \frac{n\mu\alpha}{100} \tag{17}$$

Fig.9 shows the comparison of the threshold levels in equation (15) and (17) with varying values of parameter σ and x. In Fig.9, depending on the parameter value x, the linear equation (17) gives a better threshold value I for small values of n, while the non linear equation (15) gives the better threshold value for large values of n. Calculating for the percent value of 3 σ to the μ value

$$\frac{3\sigma}{\mu}\times 100\% \tag{18}$$

As an example, applying the values from the sine oscillator circuit with σ = 0.2, and μ =17.1 gives a result of 3.5%. Using the 3 σ value is better than the fixed threshold value (percent value) because the 3 σ value can vary depending on a random variable which is the IC supply current. While low power consumption proceeds through the recent mixed signal LSI, but it has however several 10m of the electric current value.

If the fault detection is performed by the percent threshold method, the detection current value is too large in this area from Fig.9. Therefore the percent threshold method is inadequate for a fault detection. Thus, the threshold of this paper is proper to detect a fault. Because its threshold has the adaptation character (the area of large current is small threshold and the area of small current is large to the percent threshold) to the supply current value of the fault (threshold =Limit current of Fig.9).

10. The proposal of the supply current sensor

This paper proposes the current sensor to detect a fault IC to the supply current on the board. As the results of previous chapter if the supply current change, the IC is a fault.The simple supply current sensor using the window comparator is shown in the **Fig.10**.

The supply current detection resistance (Rd) and the switch is added to the + power supply terminal. This Rd is the supply current detection resistor to change the voltage to the sensor. The diode D4 is the LED to designate the fault. Applying this sensor to detect the fault in the six analog boards, the fault detection rate was shown in Table 6.

When an input voltage is between VrefL～VrefH, the output is +15V, or is outside this range, the output though is -15V, and a luminous diode switches on, and this circuit designates a fault. When a μ is a standard deviation and a σ, is a mean, normality range of the supply current I is represented as follows:

$$\mu - 3\sigma < I < \mu + 3\sigma$$

and supply current I of the normal time looks for VrefL and VrefH with the following process

(1) Rd is looked for Vcc/20<IRd<Vcc/2.

(2) (Vcc- σ Rd) +3 σ Rd=VrefH

(3) (Vcc- σ Rd) –3 σ Rd=VrefL

For example, when 741 has a σ =1.7mA and a σ = 0.2mA, here Rd=1k is taken, VrefH becomes 13.9V and VrefL becomes 12.7V.

An actual analog circuit was made with the simulation of this sensor circuit. Moreover, a fault IC and a non-fault IC were inserted, and a performance was confirmed. A voltage to set up VrefL and VrefH was decided by changing the value of the supply detection. This can be applied to the digital board as well as.

A fault at the board level can be detected by mounting two(+,－) current sensors as in Figure 10. When trouble occurs to these consumer electronic machines on the user side, a repair technician must quickly diagnose faults. After doing that, it prompts the repair technician to repair the damage in the board and the LSI level. Therefore, this sensor can be applied to the fault detection of the mixed signal LSI which will be put into digital television or another consumer electronic machines. This current sensor will be useful to these requirements.

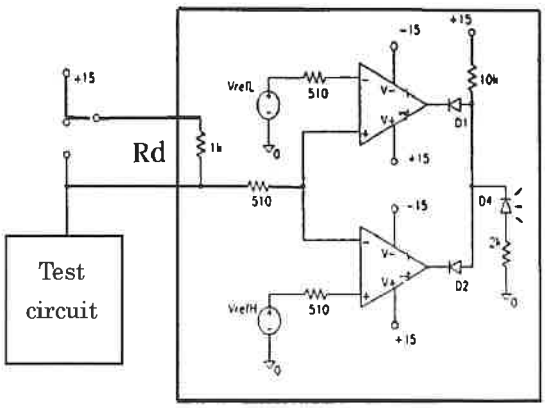


Fig.10 Current sensor.

11. Conclusion

The nine fault experiments were performed to simulate an IC Op-amp that was destroyed in the nine cases for the IC Op-Amp Fault Discussion. This paper performed the fault detection experiment using the fault transistor model. Consequently, this fact showed that an open fault and short fault includes about 91%of transistor faults. Consequently these discussions prove that the open and short transistor fault model is enough in a fault detection simulation.

The results were obtained by applying this model to six circuits using the μ A 741. Then fault detection rate obtained six boards of approximately 86% was obtained for the above mentioned six circuits. Moreover comparison of threshold level was discussed. The threshold of this paper was appropriate enough to detect a fault. From the above discussion, this paper propose the supply current sensor that can be applied to the fault detection on the user side. The results of this research, verified the usefulness of the supply current test to detect faults in analog circuits.

However, the applicability of the supply current test to detect fault ICs in other circuits aside from those tested in this paper should be verified. The next step in the research process would be to diagnose fault ICs using the supply current test if applicable or by using another method.

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